REMARKS

This Amendment is filed in response to the FINAL Office Action mailed on June 13, 2005, and in response to the Advisory Action mailed on August 31, 2005, and also in the Request for Continued Examination (RCE) filed on even date herewith. All objections and rejections are respectfully traversed.

Claims 1-20 are in the case.

No claims were amended.

Claims were added.

Please enter and consider the Amendment after Final Rejection under 37 C.F.R. 1.116 filed on August 12, 2005.

In the Advisory Action Mailed on August 31, 2005, in the continuation of Paragraph 11, the Examiner states:

"With respect to applicant's remark that Lin is completely silent regarding applicant's claimed (page 11, 1st paragraph), the examiner disagrees. Lin clearly suggest applicant's claimed in figs. 1 - 3, 5, page 4, paragraphs 37, 38, page 5, paragraphs 45, 47, page 6 paragraphs 53, 56 and page 8, paragraphs 65, 67."

This discussion relates to Applicant's arguing representative claim 1, as follows:

At Paragraphs 2-8 of the FINAL Office Action, claims 1-3 and 5-20 were rejected under 35 U.S.C. § 103 as being unpatentable in view of Lin et al. U.S. Patent Application Publication 2002/0073211 published on June 13, 2002. (hereinafter Lin)

The present invention, as set forth in representative claim 1, comprises in part:

> 1. A load balancing system for distributing tasks to a processor resource of a processor pool, the system comprising:
>
> a memory with a region organized into at least one memory block, each memory block configured to store a session;
>
> ***an interface for coupling the memory to the processor resource***, whereby the processor resource accesses the at least one memory block to update information associated with the session;
>
> ***an access monitor coupled to the interface, wherein the access monitor recognizes and tracks memory cycles associated with the at least one memory block during a specified period of time and collects statistics associated with the session; and***
>
> ***a central resource coupled to the access monitor, the central resource arranged to receive the statistics from the access monitor, and, in response thereto, to assign tasks to the processor resource.***

Applicant respectfully urges that Lin is completely silent regarding Applicant's claimed novel ***interface for coupling the memory to the processor resource...an access monitor coupled to the interface, wherein the access monitor recognizes and tracks memory cycles associated with the at least one memory block... and collects statistics associated with the session***, combined with a ***central resource arranged to receive the***

statistics from the access monitor, and, in response thereto, to assign tasks to the processor resource.

Thus, Applicant respectfully urges that Lin is completely silent concerning Applicant's claimed ***wherein the access monitor recognizes and tracks memory cycles associated with the at least one memory block.***

Lin, at the paragraphs pointed to by the Examiner, states

Lin at page 4 paragraphs 37-38 discloses:

at paragraph 37 a web browser is disclosed, along with a traffic flow rate measuring module which measures the data flow rate. The data flow rate measured is in packets, browser requests, or some other message flow parameter;

at paragraph 38 there is disclosed a webserver having a central processing unit, a cache memory, a persistent memory, and an interface to give the webserver access to information stored in the state server that pertains to sessions between users sending browser requests. The interface creates a monitoring thread between the webserver and the state server.

Lin at page 5 paragraphs 45, 47 discloses:

at paragraph 45 Lin discloses that a state table may store indicia of privileges that exist between a browser and an application server.

at paragraph 47 Lin discloses functional block diagram in Fig. 6. The diagram shows that users send browser requests to a load balancer. The load balancer distributes the browser requests to a plurality of webservers. Lin, at this point states:

"The state server 136 monitors the webservers according to their session activities and according to their availability. Once a session is initiated , a state server monitoring thread is created between the webserver and the state server to monitor and track the session occurring with the user. A monitoring thread as used here is software code application that, when executed by a processor, creates a mechanism for facilitating communication between the state server and a webserver so that the state server can send and receive signals to and from the webserver to monitor its activities. The state server can then determine whether the webserver is in service during a session between an application server and a browser. If that connection ever terminates, the state server will have retained relevant session information so that an application server may attempt to reconnect and possibly get rerouted to another webserver to continue a session"

Lin at page 6 paragraphs 53, 56 discloses:

Lin at paragraph 53 discloses a load balancer which routes a browser request to a webserver. Lin states:

"Using the traffic flow rate measure 204, the load balancer chooses an available webserver and routes the browser request to the webserver with the webserver interface 206."

Lin at page at page 8 paragraphs 65, 67 discloses as follows:

Lin at paragraph 65 discloses that an application server transmits a heartbeat signal to a webserver, in order for the webserver to know that the application server is alive.

When the webserver does not receive the heartbeat signal, the webserver marks the socket as invalid, and returns to monitoring the application server.

Applicant respectfully urges that nowhere in the cited paragraphs of Lin is there any disclosure of Applicant's claimed novel ***wherein the access monitor recognizes and tracks memory cycles associated with the at least one memory block.***

That is, Applicant claims ***wherein the access monitor recognizes and tracks memory cycles***

and Lin is silent concerning ***monitoring memory cycles***.

Thus, Applicant respectfully urges that Lin is completely silent concerning Applicant's claimed ***wherein the access monitor recognizes and tracks memory cycles associated with the at least one memory block.***

Further, the Examiner states in the continuation of paragraph 11 of the Advisory Action:

"Regarding applicant's remark that Lin is completely silent regarding applicant's novel technique for determining processor load based on memory activity (page 11, 2nd paragraph, 3rd sentence), applicant is arguing a feature of the invention not specifically stated in the claim language, which is improper."

Applicant respectfully urges that Applicant claims, as shown by representative Claim 1, the novel ***interface for coupling the memory to the processor resource...an access monitor coupled to the interface, wherein the access monitor recognizes and tracks memory cycles associated with the at least one memory block... and collects statistics associated with the session***, combined with a ***central resource arranged to receive the statistics from the access monitor, and, in response thereto, to assign tasks to the processor resource.***

Accordingly, Applicant respectfully urges that representative Claim 1 is allowable because Lin is silent concerning Applicant's claimed novel ***wherein the access monitor recognizes and tracks memory cycles***.

In a review of Lin, applicant was unable to find a statement by Lin that Lin monitors ***memory cycles***. Lin simply monitors traffic to and from a webserver.

Further, Applicant respectfully urges that Applicant's claimed novel concept of monitoring ***memory cycles*** is totally different from Lin's concept of monitoring traffic to and from a webserver, and that the two concepts are patentably distinct.

Accordingly, Applicant respectfully urges that Lin is legally precluded from rendering unpatentable Applicant's claimed novel invention under 35 U.S.C. 103(a) because of the absence from Lin of Applicant's claimed novel ***interface for coupling the memory to the processor resource...an access monitor coupled to the interface, wherein the access monitor recognizes and tracks memory cycles associated with the at least one memory block... and collects statistics associated with the session***, combined with a ***central resource arranged to receive the statistics from the access monitor, and, in response thereto, to assign tasks to the processor resource.***

All independent claims are believed to be in condition for allowance.

All dependent claims are dependent from independent claims which are believed to be in condition for allowance. Accordingly, all dependent claims are believed to be in condition for allowance.

Favorable action is respectfully solicited.

Please charge any additional fee occasioned by this paper to our Deposit Account No. 03-1237.

Respectfully submitted,

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